500 Million Transistor Integrated Circuit Delay Analysis : Parameter Optimization using Taguchi Approach

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Abstract

Delay analysis of 500 million transistor integrated circuit is optimized using test plan L8, in the form of an orthogonal array and a software for automatic design and analysis of experiments both based on Taguchi approach. Optimal levels of physical parameters and key components namely number of metal layers, minimum feature size, resistivity, threshold voltage, effective length, saturation drain current and supply voltage play an important role in the estimation of integrated circuit frequency. The chip frequency under these optimal conditions was 2472.85MHz.

Keywords*: Delay analysis, Optimization, Taguchi method, Chip Frequency*

1. Introduction

Diminishing feature sizes and increase in chip size has made interconnect a key factor to be optimized in order to achieve area and performance targets. Excessive factorization and inordinate attention to active area minimization favors selection of high fan in gates and unbalanced decompositions of paths which in turn lead to increase in routing congestion, increase in wire lengths, delay and consequently degradation in performance and decrease chip frequency. In recent years, power dissipation has become a critical design concern that needs to be optimized along with area and speed. Fabrication technology moved very fast, in the last few years from 0.1 μm to 45 nm process with simultaneous availability of additional routing layers. Reducing the number of vias, net lengths, metal migration effects are main concerns with high speed designs. Signal integrity is becoming a serious factor in determining the reliability and performance of electronic systems. For circuit analysis and synthesis, several delay models are proposed. [1 – 4]. For high speed circuits, the duration between input transitions might be comparable to circuit delays such as in wave pipe lining Circuits [4].

In conventional optimization procedures, one parameter is altered at a time while keeping the other parameters constant, to understand the impact of that particular parameter. Although several processes have been optimized using this methodology, these optimization procedures are time consuming and cannot provide the information on mutual interactions of the parameters on the desired outcome. Statistical procedures have advantages over conventional methodologies in predicting the accurate results basically due to utilization of fundamental principles of statistics, and randomization. One of the popularly used optimization procedures is response surface optimization (RSM) mainly developed based on full factorial central composite design. Other one genetic algorithm and Manto Carlo techniques. Wire sizing with buffer placement and sizing for power delay trade offs, scaling of VLSI parameters have been optimized using this methodology. However this statistical experimental design is only related with the number of variables but is not related to statistical factorials.

Recently developed Taguchi method based on orthogonal arrays provides three phases of off line quality control (i.e. system, parameter and tolerance design). System design helps to identify the working levels of design factors while parameter design indicates the factor level that

gives the best performance of the product / process under study, whereas tolerance design helps in fine tuning the tolerance of the factors that significantly influence the product formation. This Taguchi method not only helps in considerable saving in time and lost but also leads to a more fully developed process. It has several design arrays such as OA12, OA18, OA36 and OA54, which enable a focus on main effects and helps in increasing the efficiency and reproducibility of small scale experiments [5-8].

Many Japanese manufacturers have used the Taguchi Approach and improved product and process qualities with unprecedented success. It created significant changes in several Industrial organizations in the USA and Europe. In present Communication, the authors have optimized delay analysis of 500 million transistor chip by Taguchi methodology. The effects of eight variables, number of metal layers, minimum feature size, resistivity, threshold voltage, effective length, saturation current, supply voltage, oxide thick ness on delay analysis has been done using the software Qualiteck 4 [9-11].

2. Methods

2.1 Statistical timing analysis

It [12, 13] has been used along with block oriented path tracing to ensure the timing performance of a circuit. STA takes the variation of fabrication process into consideration and provides designers a probability distribution of the longest path delay. There are several ways to find a probability distribution of the longest path delay of a circuit.

The first method is based on the PERT like [13] approach which approximates the real probability distribution of the path with the largest mean delay. This distribution is accurate when these exists only a few dominant long paths in a circuit, not a high performance VLSI circuit. The second method is to perform extensive simulation of some circuits and fit the results to some known probability distributions [15]. The third method is to perform statistical timing simulation. This method can generate a fairly accurate probability distribution of the longest path delay when a large number of experiments are performed. However, it is computationally intensive for a large VLSI circuit.

In the present work a model has been formulated to compute chip frequency of the 500 million integrated circuit [15-20]. The higher performance in ASIC is quantified by the clock speed, for this critical path is identified. Inter connect effects will dominate the performance. Incorporating new materials specifically copper wiring and low K dielectrics, and increased packing density on a chip with smaller wiring lengths will help in increased chip frequency. Device and inter connect characteristics, local wire lengths, gate delays and inter connect delays are determined. Using inter connect characteristics, R and C at each level is computed. Device resistance, junction and input capacitances calculated using device characteristics. Wiring analysis will be done along with optimizing gate width.

Clock frequency is effected by process variation, skew, latch hold time, logic delay, critical path and global delay. Feature size will help in setting metal line widths, dielectric constants etc. Pitch, line thick ness and material properties are estimated. The analytical capacitance formulae are based on [15].

Local routing is done on lower level metals. The junction and input device Capacitances are defined. An effective device resistance for delay is also computed. The device resistance is more significant than the line resistance. The output device capacitance together with the wiring capacitance and fan out capacitance are computed giving a single load capacitance.

The device resistance is defined as

$$R_{dev} = \frac{0.806\, V_{dd}}{I_{dsat}} \qquad (1)$$

Driver resistance is also calculated, that relates a device current and voltage relationship directly to effective resistance. The network viewed as lumped RC system.

The input capacitance of device is expressed as

$$C_{in} = C_{ox} + C_{overlap} \quad (2)$$

Wire length modeling is generally based on Rent's rule is given by

$$T = K (N_g)^p \quad (3)$$

In this expression, T denotes number of terminals or signal pins; K is a factor accounting for the number of pins per gate. N_g is the number of gates in the circuit and p is the Rent's exponent.

By comparing the external communication requirements of different size blocks, the average wire length can be determined and is used for wire length estimation models [17]. The average wire length is given by

$$L_{avg} = P_g R_{avg} \quad (4)$$

Here P_g is the gate pitch in microns and R_{avg} is the number of gate pitches that an average wire must traverse and is determined from Donath's model.

In order to limit the impact of inter connect on performance, driving gates should be sized properly. Critical length is given by

$$L_{crit} = \sqrt{\frac{0.693\, R_{dev}\, C_{dev}}{0.377\, R_w\, C_w}} \quad (5)$$

Gate delay for fixed fan out is

$$T_{delay} = 0.377 R_w C_w + 0.693 [R_{dev}(C_j + C_{in}) + R_{dev} C_w + R_w C_{in}] + T_{din} \quad (6)$$

The total chip delay is

$$T_{cycle} = T_{logic} + T_{global} + T_{setup} + T_{latchdey} \quad (7)$$

2.2 Design of experiments

Taguchi has established OAs to describe a large number of experimental Situations mainly to reduce experimental errors and to enhance the efficiency and reproducibility of laboratory experiments. The symbolic designation of these arrays indicates the main information on the size of the experimentation e.g. L8 has 8 trials. The total degree of freedom available in an OA is equal to the number of trials minus one. Each column consists of a number of conditions depending on the levels assigned to each factor. In the present study, all eight columns are assigned with different factors as indicated in table 1. each factor is assigned with two levels. Table 2 shows the layout of the L8 (2^7) OA used in the present study. Using the assigned parameter values the simulations are performed and listed in table 2.

3. Software Package

Qualiteck 4 and MATLAB softwares for automatic design and analysis of Taguchi experiments was used to study the following objective of the analysis

1. Determination of optimum conditions
2. Estimation of performance at the optimum condition

4. Analysis of results

Optimum conditions for achieving maximum chip frequency and corresponding chip area is given in table 3 .The ANOVA for this conditions is shown in table 4. These results suggest that influence of one factor on chip frequency and chip area was dependent on conditions of other factors in optimizing the chip frequency.

5. Conclusion

The combination of factors that are influencing the highest chip frequency are identified. The Taguchi approach has proved in optimization of chip frequency and estimation of corresponding chip area.

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Table 1

Factors and their levels assigned to different columns

Serial number	factor	level 1	level 2
1	Number of metal Layers	8	9
2	Minimum feature Size (μm)	0.07	0.05
3.	Resistively (μΩ- cm)	2.2	3.5
4.	Threshold voltage (V)	0.225	0.125
5.	Effective length (nm)	35	25
6.	Saturation current (μA/μm)	600	400
7.	Supply voltage (V)	0.9	0.8

Table 2

L8 (2^7) OA

Experiment number	column							chip Frequency MHz	chip area mm^2
	1	2	3	4	5	6	7		
1	1	1	1	1	1	1	1	2002.69	530.08
2	1	1	1	2	2	2	2	1780.98	530.08
3	1	2	2	1	1	2	2	1472.85	270.45
4	1	2	2	2	2	1	1	2230.27	270.45
5	2	1	2	1	2	1	2	2312.09	530.08
6	2	1	2	2	1	2	1	1557.42	530.08
7	2	2	1	1	2	2	1	1589.17	270.45
8	2	2	1	2	1	1	2	2442.09	270.45

Table 3
Optimum conditions

Serial number	Factors	Level	Level description
1	Number of metal layers	1	8
2	Minimum feature size	2	0.05
3	Resistivity	2	3.5
4	Threshold voltage	1	0.225
5	Effective length	1	35
6	Saturation current	2	400
7	Supply voltage	2	0.8

Expected result at optimum conditions, chip frequency is 2472.85 MHz & chip area 270.45mm^2

Table 4
ANOVA

Source	SS	DF	MS	F
Columns	1671579.6	6	278596.6	170.2
Error	80205.4	49	1636.8	
Total	1751785	55		

References

1. W.K.C. Lam and R.K. Brayton," Timed Boolean functions" Kluwer academic publisher,USA, 1994.
2. C.T. gray, W. Live and R. K. Cavim, III," Timing constraints for wave pipelined systems", IEEE trans. CAD, VOL 13, No.8, August 1994.
3. H.C.Chen and D.H. Du," path sensitization in critical path problem," 1990 ACM Workshop on timing issues in the specification and synthesis of digital systems, 1990.
4. S.Devadas, K.Keutzer and S.Malik ," computation of floating mode delay in Combinational circuits: theory and algorithms," IEEE trans. CAD VOL 12, No.12, Dec 1993.
5. Joseph J, Piganatiells JR." An overview of the strategy and tactics of Taguchi, " IIE Trans 1988;20: 247-53.
6. Rajesham S, Jerm cheong J. A study on the surface characteristics of burnished components" J Mech working technology 1989 : 20: 129 – 38.
7. Rajesham S, K. Jaya kumaran, K.Ullah, J.Miller, J M D'Sullivan, S.Arunachalam, "process capability analysis for producing high percision. Cylindrical bores using ballisting and super abrasive as a joint technique – Taguchi approach". International conference on quality engineering and management, 4–6thAugust coimbatore, India, 1997, pp501 – 506.
8. Roy R K " A primer on the Taguchi method", Society of manufacturing Engineers,1990.
9. G .Smith, "Model for delay faults based upon paths: in process of ITC, pages 342 – 349,Nov 1985.
10. S.S.Sapatnekar," RC inter connect optimization under the elmore delay model," in proc DAC,PP,387-391,1994.
11. H.B.Bakoglu, circuits,inter connections and packaging for VLSI Reading MA: AddisonWesley,1990.
12. Jacques Benkoski and Andrei J Strojwas "New Techniques for statistical timing simulator" the ACM/IEEE 23th Design automation conference, 1986, pp134-137.
13. J. I. Kirk Patrick and N. R. Clark " PERT as an AID to logic design", IBM journal, March 1966, PP 135 – 141.
14. D. R. Tryon, F. M. Armstrong and M. R. Reiter, " Statistical failure analysis of system timing", Journal of research and development, vol 28, No.4, July 1984, PP 340 –355.
15. J. H. Chern, J. Huang, L. Arledge P. C Li and P. Yang " Multi level metal capacitance models for CAD design synthesis systems", IEEE electron device letters vol 13, PP 32 – 34, Jan 1992.
16. D. Sylvester, O. S. Nakagawa and C. Hu " Modeling impact of back end process variation on circuit performance," submitted to international solid state circuits conference, 1999.
17. W. E. Donath " Placement and average inter connection lengths of computer logic", IEEE transactions on circuits and systems, vol 26 , PP 272 – 277, April 1979.
18. R .W. Keyes " The wire limited logic chip" IEEE Journal of solid state circuits ,vol 17, PP 1232 – 1233, Dec 1982.
19. T. Sakurai " Closed form expressions for inter connection delay , coupling and cross talk in VLSI ," IEEE transaction on electron devices vol 40 , PP 118 – 124, Jan 1993.
20. T. Sakurai, A. R. Newton "Alpha power MOSFET model and its applications to CMOS inverter delay and other formulae," IEEE Journal of Solid state circuits, vol 25 ,PP 584 – 594, April 1990.

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