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STUDY AND SIMULATION OF SILICON NANOWIRE FIELD EFFECT TRANSISTOR AT SUBTHRESHOLD CONDITIONS USING HIGH K DIELECTRIC LAYER AT ROOM TEMPERATURE

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Abstract:
This paper discuss about the simulation of silicon nanowire field effect transistor with different dielectric materials like Sio_2 , Hfo_2, Zro_2 and High k dielectric material like salt water. The performance of silicon nanowire transistors at 300K, 77K and 325 K are also studied. We have simulated ballistic silicon nanowire transistor by considering simple analytical approach. Subthreshold conditions like Drain induced barrier lowering, Threshold swing, switching speed, Ion and Ioff currents are studied for each dielectrics. We conclude that High k dielectric layer can be used to increase the performance of silicon nanowire transistor at room temperature. Gate and drain control parameters can be used to suppress the harmful subthreshold conditions. We also simulated silicon nanowire transistors by varying the gate control parameter and study the results from the simulation. We have used fettoy and nanomos simulators for this study.
Keywords:
Drain Induced Barrier lowering DIBL, Threshold Swing, Silicon Nanowire transistor, Quantum capacitance limit.

1. Introduction

As the conventional silicon MOSFET scaling approaches its scaling limit, new device structures are being investigated and explored. Among them silicon nanowire has attracted broad attention among the industries as future nanodevice. Hence the study of performance limit and scaling limit of silicon nanowire transistors and the behavior of silicon nanowire at subthreshold condition are discussed in this paper. The essential physics of silicon nanowire transistors are electrostatics, transport and band structure. A full three dimensional, self-consistent, ballistic SNWT simulator has been developed based on the effective-mass approximation and study the performance limits of SNWTs with their device physics are given in detail in [1] The device scaling has been successfully predicted by Moore's law [2] – the number of transistors on one IC chip has quadrupled every three years and the feature size of each transistor has shrunk to half of its original value at the same time. Continued success in device scaling is necessary for maintaining the successive improvements in IC technology. As the MOSFET gate length enters the nanometer regime, however, short channel effects (SCEs) [3], such as threshold voltage (*VT*) rolloff and drain-induced-barrier-lowering (DIBL), become increasingly significant, which limits the scaling capability of planar bulk or silicon-on-insulator (SOI) MOSFETs. At the same time, the relatively low carrier mobility in silicon (compared with other semiconductors) may also degrade the MOSFET device performance (e.g., ON-current and intrinsic device delay). For these reasons, various novel device structures and materials like silicon nanowire transistors [4], [5], [6] molecular transistors are being extensively explored. A rigorous simulation of SNWTs requires the treatment of 3D electrostatics, 2D quantum confinement and 1D quantum transport.[1] In this work, the 3D Poisson equation is considered for simulation and solved by the finite element method [7][8] that begins by solving for electron subbands slice by slice along the nano wire. We use fettoy simulator [9] for simulation of silicon nanowire and study the device metrics at subthreshold condition. The device metrics considered are

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Drain induced barrier lowering (DIBL), threshold swing, on – off current, voltage gain, threshold roll off, Intrinsic device delay, switching speed from Ion / Ioff ratio and transconductance. These parameters are helpful to study the subthreshold condition in silicon nanowire transistors. We also simulated silicon nanowire at different temperatures, dielectrics, different gate and drain control parameters. Figure 1 shows the structure of silicon nanowire transistor.

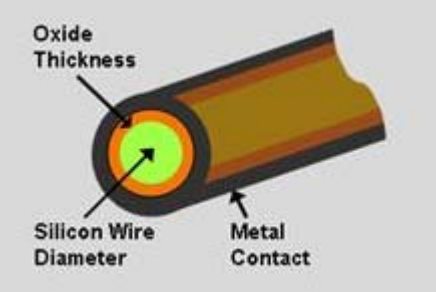

Figure 1 structure of silicon nanowire transistors with oxide thickness and metal contact [9]

2 Simulation approach

We have simulated silicon Nanowire FET (SNWFET) by using the simple analytical approach. A coaxial gate geometry configuration is assumed and the channel is <100> oriented, so the valley degeneracy is 4 M = 4 (.e., the four valleys, [ ] 010, 010 . . . . , [ ] 001, and 001 . . . . , are degenerate) and the longitudinal effective mass is * 0.19 *x e m* A hypothetically thin silicon body, 5 *nm* is selected to guarantee that only the lowest sub band at each valley is occupied. Moreover, we assume the oxide layer thickness of 5 *nm* and four different oxide layers are selected to illustrate the full-degenerate and quantum capacitance effects in nanowire FETs. To capture the 3D electrostatics in the simulated nanowire FETs, we assume that gate control parameter as 0.88 [5] and drain control parameter as 0.035. We studied the simulation at room, high and low temperatures. Finally for different drain and gate control parameters, the sub threshold effects of nanowire transistors are studied. Table 1 consists of input parameters for the fettoy simulators (set of matlab programs for

Table 1 input parameters for the simulation using Fettoy and Nanomos – 2.5 simulators

S.NO	INPUT PARAMETERS	VALUES USED IN THE SIMULATION
1	Insulator thickness	1.50e-009 m
2	NanoTube Diameter	1.00e-009 m
3	Insulator relative dielectric constant	3.90 & 80
4	Temperature	300.00 K & 77 k
5	Initial source Fermi Level	-0.320 eV
6	Gate control parameter	0.880 (0.2 – 0.98)
7	Drain control	0.035
8	Voltage Loop (for both Vgs and Vds):	Initial Bias VI=0 V Final Bias VF= 1.000V

simulating the silicon nanowire transistors). We have drawn drain current versus gate voltage and drain voltage of silicon nanowire transistors. We have studied quantum capacitance effect from Quantum capacitance versus gate voltage characteristics of silicon nanowire field effect transistor. We compared gate insulator capacitance and quantum capacitance of the devices and come to

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conclusion that device is in quantum confinement limit and also discussion about these curves at full degenerate (high gate bias) and no degenerate (low gate bias limits) conditions. Table 2, 3 gives simulated values of silicon nanowire transistor.

Table 2 output values of silicon nanowire FET at different temperature and gate control parameter.

Output Parameters	Silicon Nanowire MOSFET at 300 K	Silicon Nanowire MOSFET at 77k	Silicon Nanowire MOSFET at 325 K	Silicon Nanowire MOSFET at 0.8 GCP	Silicon Nanowire MOSFET at 0.5 GCP	Silicon Nanowire MOSFET At 0.92 GCP
Ion	2.049e-005	2.035e-005	2.062e-005	1.844e-005	9.179e-006	2.149e-005
Ioff	6.611e-011	1.456e-012	1.671e-010	6.611e-011	6.611e-011	6.611e-011
Threshold swing (S) mv /dec	67.72	32.28	73.59	74.67	111.19	67.65
DIBL mv / v	41.15	20.43	41.66	45.24	72.30	41.33
Transconductance gm (S / m)	4.337e-005	4.048e-005	4.238e-005	3.915e-005	2.561e-005	4.563e-005
Output conductance, gd (S/m)	1.852e-006	1.945e-006	1.794e-006	1.816e-006	1.904e-006	1.868e-006
Voltage gain at highest gate and drain bias, Av	25.42	24.41	23.63	21.56	13.45	25.42
Carrier injection velocity m/s	2.489e+005	2.467e+005	2.508e+005	2.378e+005	1.849e+005	2.545e+005
Ion / Ioff ratio	0.3e006	13.96e006	1.2e005	2.7e005	1.3e005	3. 2e005

Table 3 output values of silicon nanowire FET using different dielectric

S.No	Output Parameters	Silicon Nanowire With sio2 as dielectric (3.9)	Silicon Nanowire MOSFET With Zr0 (15)	Silicon Nanowire MOSFET With Hfo2 as dielectric (25)	Silicon Nanowire MOSFET with high k dielectric(salt water = 80)
1	Ion	2.696e-005	6.573e-005	7.524e-005	8.661e-005
2	Ioff	6.611e-011	6.611e-011	6.611e-011	6.611e-011
3	Threshold swing (S) mv /dec	67.97	67.90	67.77	67.75
4	DIBL mv / v	41.15	35.76	-118.68	-16235.16
5	Transconductance gm (S / m)	6.034e-005	1.124e-004	1.220e-004	1.320e-004
6	Output conductance, gd (S/m)	2.510e-006	4.501e-006	4.870e-006	5.257e-006
7	Voltage gain at highest gate and drain bias, Av	24.42	24.97	25.05	25.11
8	Carrier injection velocity m/s	2.852e+005	4.441e+005	4.746e+005	5.088e+005
9	Ion / Ioff ratio	4.07e005	9.9e05	11.38e005	13.1e005

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3 Results and Discussions

3.1 Silicon Nanowire FET -Quantum Capacitance and Gate voltage charecteristics Qc Vs V_{gs}

The quantum capacitance Qc plays significant role in comparing with gate oxide capacitance Cg. When Cg is much greater than Qc, it can be shown that device can be operated near to Quantum Capacitance Limit. When the device is in quantum confinement limit, C-V curves at full degenerate (high gate bias) and no degenerate (low gate bias limits) are investigated. Figure 2 shows the Quantum capacitance and gate voltage of silicon nanowire transistors with different dielectric. At low voltage limits (0 – 0.45 volts no degenerate conditions) the value of Qc is 0.7 nf for Hfo2 dielectric and at higher voltage limits 0.45-1 volt the quantum capacitance value falls down 0.4 nf for high k dielectric. So quantum capacitance value at full degenerate condition is lower than no degenerate condition. It is proved in [1,5] nanodevices to be operated near to quantum confinement limit, quantum capacitance limit has to be lower at higher voltage than at lower voltage. Figure 2 shows the Qc-Vg curve with different dielectric layers, it shows high k

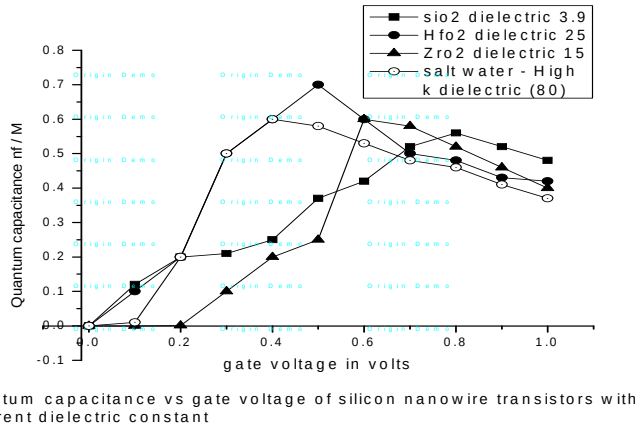

Figure 2 Quantum capacitance vs. gate voltage of silicon nanowire FET

dielectric material has higher lower limit voltage around 0.5-0.6 volts and lower quantum capacitance of 0.4 nf at 1 volt than other dielectric curves. High k dielectric layer has well defined capacitance curve, and also it shows better accumulation, depletion and inversion regions. Figure 3 shows Qc-Vg curves at different gate control parameters. In silicon nanowire transistors gate and drain control can be done for suppressing shot channel effects. It is proved in [4,5,7] gate control parameter of 0.88 and drain control parameter of 0.035 can be used to model the silicon nanowire transistors. Gate control parameter is the ratio of gate capacitance to sum of gate, source and drain capacitance. From figure 3 increasing the ratio by 0.4 which decreases the quantum capacitance for 0.92 gate control parameter.

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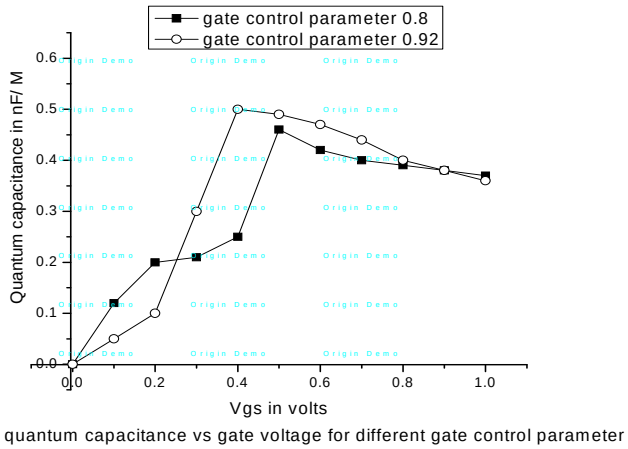

Figure 3 Quantum capacitance vs. gate voltage of silicon nanowire FET for different gate control parameter.

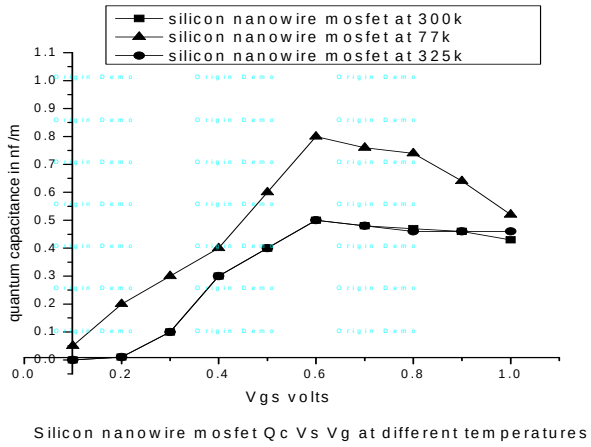

Figure 4 shows Qc- Vg curve at different temperature.

Figure 4 shows the Qc-Vg curves at different temperatures. At room temperature Quantum capacitance value at higher voltage is 0.4nf and better than 77k and 325 k curves. We conclude that high k dielectric with higher gate control parameter at room temperature can be used to decrease the quantum capacitance.

3.2 Ids – Vds, Vgs characteristics.

Figure 5, 6, 7 shows the Ids – Vds characteristics at constant Vgs = 1 volt. As the gate voltage increases the channel conductance also increases but at full degenerate condition the source Fermi level is well above the top of the barrier, the channel conductance saturates to fixed value. Now the device enters into the full degenerate condition near to quantum confinement. Design equations and explanation about IV- curves are given in [5,7]. Figure 5 shows Ids – Vds characteristics at constant Vgs = 1 volt, high k dielectric and Sio_2 curve saturates at higher gate bias than other dielectric curves. The reason is high k dielectric layer and Sio_2 shows full degenerate at higher bias from 0.65 to 1 volt and channel conductance saturates at higher voltage limits. Moreover high k dielectric curve saturates at higher drain current of 89 micro amps and hence higher on current when comparing sio_2 curve. Figure 6 shows the Ids – Vds curve at 0.8, 0.92 gate control parameter.

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Gate control parameter of 0.92 curves has higher drain current 30 micro amps and saturates at higher gate voltage of 0.67 volts. Figure 7 shows the Ids – Vds curve of silicon nanowire field effect transistor at different temperatures. The room temperature curve saturates at higher drain current of 24 micro amps at higher gate bias of 0.65 volts when compared to 77 and 325 k curves.
Figure 8,9,10 shows the Ids vs Vgs at constant Vds of 1 volt. From figure 8 high k dielectric curve has higher drain current 90 micro amps and higher threshold around 0.62 volts than other dielectrics. Figure 9 shows the simulation of silicon nanowire transistors at 0.8 and 0.92 gate control parameters. Higher gate control provides higher current at higher gate bias with low leakage. Figure 10 shows Ids vs Vgs at different temperatures. At room temperature higher gate bias of 0.62 volts and higher drain current around 25 micro amps comparing 77, 325 curves. We conclude that high k dielectric as dielectric layer and higher gate control of 0.9 at room temperature has low leakage current (0.1 nanoamps), higher gate bias; higher drain current than other parameters mentioned. So it is desirable to have high k dielectric layer at room temperature on single silicon nanowire transistors.

3.3 Sub threshold parameters

Device metrics at sub threshold regions are Threshold swing, Drain induced barrier lowering DIBL, I_{on} / I_{off} current, Switching speed and intrinsic delay. Device physics and design equations of nanowire transistors are given in detail in [1] Table 2 and 3 shows the single silicon nanowire transistor output values of the fettoy simulator. As temperature increases Ion on current also increases and at higher gate control higher on current of 21.4 micro amps is noted down. Lower DIBL, Threshold swing, Ion / Ioff ratio (higher Switching speed) and intrinsic delay are the subthreshold parameters needed for the best results. At 77 k and 0.92 GCP low DIBL of 32.28 and 67.65 and threshold swing of 20.4 and 41.33 are noted down. But 77 k has lower voltage gain and at room temperature voltage gain and subthreshold parameters are better compare to 325 k temperature. The intrinsic delay for sio_2 curve is 0.09 pico second. Switching speed is better for 325 k temperature and 0.5 GCP. Table 3 shows the sub threshold parameters using different dielectric of silicon nanowire transistor. High k dielectric has highest on

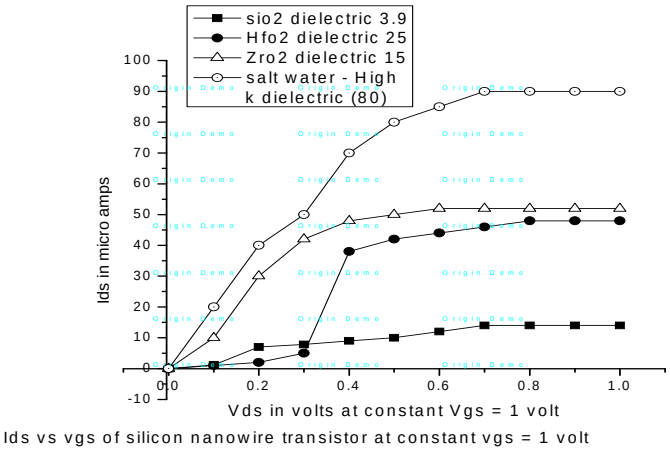

Figure 5. shows the Ids vs Vgs of silion nanowire transistor with different dielectric

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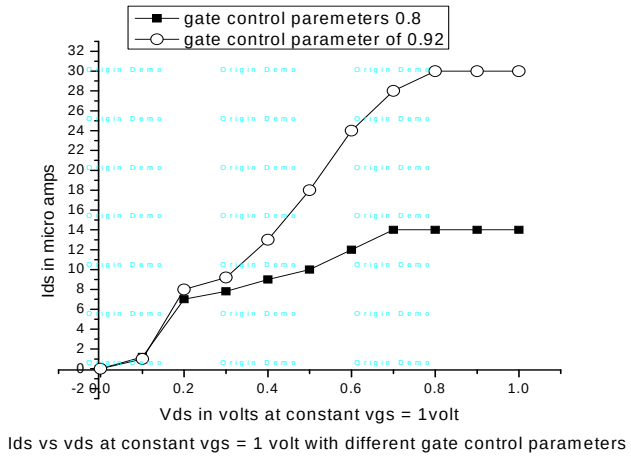

Figure 6. Ids vs. Vds with 0.92,0.8 gate control parameters

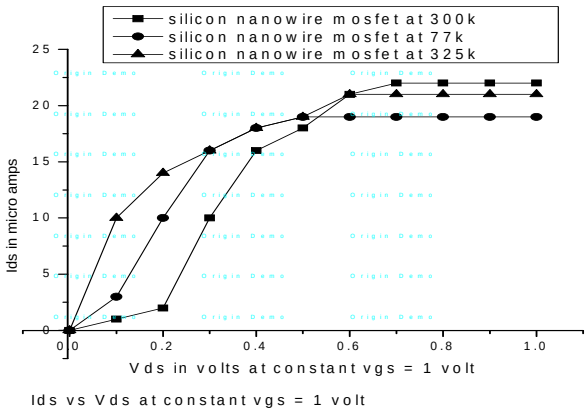

Figure 7. Ids vs Vds at different temperatures

current, lower DIBL and threshold swing than other dielectrics used.

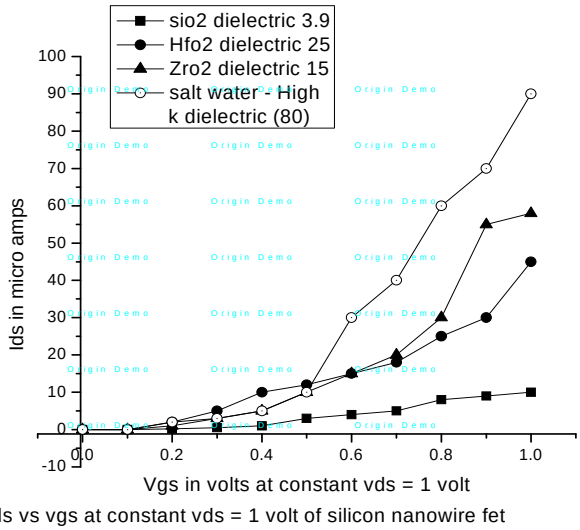

Figure 8. Ids vs Vgs of Silicon nanowire transistor at constant Vds = 1 volt

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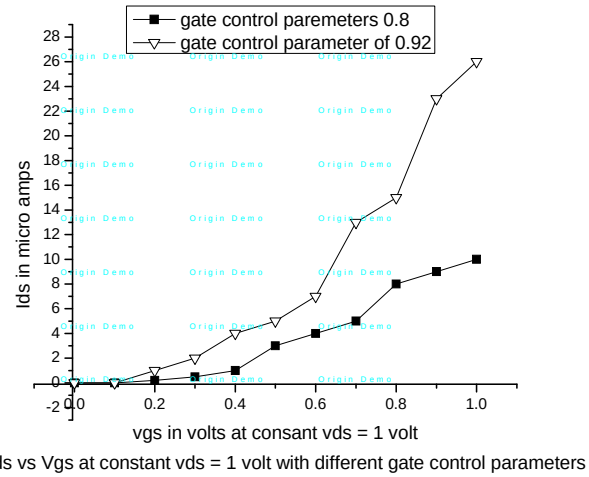

Figure 9. Ids vs Vgs at different gate control parameter of silicon nanowire transistor

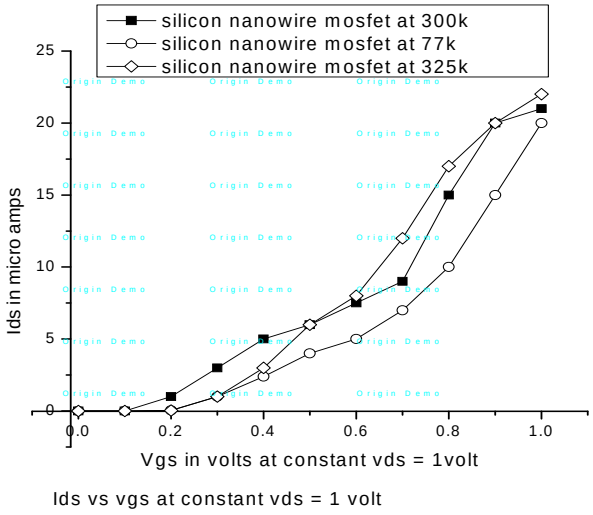

Figure 10. Ids vs Vgs of silicon nanowire transistors at different temperature.

3.4 Transconductance, Voltage gain, Carrier injection velocity

At room temperature and gate control parameter of 0.92 silicon nanowire transistor has highest transconductance of 4.337 e-5 S/m and 4.63 e-5 S/m and highest voltage gain of 25.42 comparing other parameters. The carrier injection velocity at 0.92 GCP has 2.545 e05 m/s. The transconductance of high k dielectric is 1.32 e-4 S/m, and highest voltage gain of 25.11 and carrier injection velocity of 5.088 e05 m/s.

4.0 Conclusion

1. High k dielectric layer can be used to increase the performance of silicon nanowire transistors at room temperature using 3D electro statistics of 0.92 gate control parameter.
2. High K dielectric has lower quantum capacitance at higher gate voltage and operated near to quantum capacitance limit.
3. High k dielectric layer and higher gate control parameter has higher on current, transconductance and voltage gain.
4. High k dielectric layer and GCP of 0.92 has low DIBL, Threshold swing, Intrinsic delay and higher switching speed which can be used to suppress the subthreshold effects in nanodevices.

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