INVESTIGATION AND USAGE OF NOVEL CHANNEL MATERIALS FOR THE SIMULATION OF SILICON NANOSCALE MOSFET

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Abstract:

This paper discuss about the simulation of ballistic nanoscale Mosfet by considering the device physics of charge control and quantum confinement limits. As the MOSFET scaling enters the nanometer regime, short channel effects which increases significantly and limits the scaling capability of MOSFET. We have investigated the different channel materials on silicon nanoscale mosfet and study its subthreshold parameters. The device metrics considered at the nanometer scale are subthreshold swing, Drain induced barrier lowering, on and off current, carrier injection velocity and switching speed. Fettoy simulator is used for the simulation and the parameters calculated and tabulated. We have drawn capacitance and gate voltage, drain current and drain – gate voltage characteristics with different channel materials of nanoscale silicon MOSFET. The channel materials in the simulation considered are strained silicon, germanium, Gallium arsenide (GaAs) and Indium arsenide (InAs). Strained silicon has less subthreshold effects, higher voltage gain and lower threshold swing; germanium has higher on current and carrier injection velocity. Strained silicon on germanium channel material has capability

Keywords: Threshold swing, Drain induced barrier lowering, Subthrehold effects, ballistic transistors, nanoscale MOSFET.

1. Introduction

The performance of ballistic nanoscale mosfet can be improved by considering different channel material like germanium, Gallium arsenide (Ga As), Indium arsenide (In As) and strained silicon. The gate length of the MOSFET is scaled down from 100 um to 35 um. As scaling of MOSFET continues, its steady performance shows that it is a leading technology for high performance and low power applications. Due to leakage current issues and oxide reliability, the thickness of oxide layer can be scaled down to 1 nm only. Beyond that we need to have high k dielectric material as replacement for silicon dioxide. SI-Sio₂ has excellent interface property, but silicon has poorest transport properties like mobility and diffusion constant, so study of the alternative material can be considered for the channel region.[1] [2]

We have simulated ballistic silicon nanoscale mosfet with different channel materials. There is considerable interest these days in exploring the use of alternative channel materials such as Ge, GaAs, and InAs.We have considered strained silicon, germanium

(Ge), Gallium Arsenide (GaAs) and Indium Arsenide (InAs) materials as channel for silicon nanoscale MOSFET. Table 1 shows the input parameters for the simulation work. Apart from the table 1 we have considered different valley degeneracy and effective mass of germanium, GaAs and InAs. The performance advantage and device metrics of these devices are studied from the simulation work. We have Compared the on-currents of ballistic strained silicon, germanium, gallium arsenide, and indium arsenide n-MOSFET in (110). For this calculation, we used 1D electrostatics (gate control parameter = 1 and drain control parameter = 0) Assume VDD = 1.0V, room temperature operation, and selecting the appropriate effective mass and valley degeneracies for each case.

	chamer materials using retoy and realonios – 2.5 simulators								
		Strained Silicon as	Germanium as	GaAs as channel					
S.NO	INPUT	channel material for	channel material for	material for silicon	InAs as channel				
	PARAMETERS	silicon nanoscale	silicon nanoscale	nanoscale MOSFET	material for silicon				
		MOSFET	MOSFET		nanoscale MOSFET				
1	Insulator thickness	5.00e-9	5.00e-9	5.00e-9	5.00e-9				
3	Insulator relative	3.9	3.9	3.9	3.9				
	dielectric constant								
4	Transport	0.19	0.08	0.063	0.028				
	Effective mass								
4	Temperature	300 K	300 K	300 K	300 K				
5	Initial source	-0.32 ev	-0.32 ev	-0.32 ev	-0.32 ev				
	Fermi Level								
6	Gate control	1.00	1.00	1.00	1.00				
	parameter								
7	Drain control	0	0	0	0				
8	Voltage Loop (for	Initial Bias VI=0 V							
	both Vgs and	Final Bias VF=	Final Bias VF=	Final Bias VF=	Final Bias VF=				
	Vds):	1.000V	1.000V	1.000V	1.000V				

Table 1 input parameters for the simulation of nanoscale MOSFET with different channel materials using Fettov and Nanomos – 2.5 simulators

2.Simulation approach

A general theoretical approach for the quantum mechanical simulation of nanoscale mosfet with non equilibrium green's function is given in detail in [1]. The tightly bonded model and quasi 3D ballisitic model have revealed important trends in deeply

Scaled new channel material devices. These models are explained in [3.] [4]

Table 1 shows the input parameter for our simulation. Table 2 shows the results of the simulation.

3.Results and discussions

Strained silicon has Ion current of 3.273 milli amps and highest off current among other materials 1.732 micro amps. So by comparing the strained silicon with other materials in table 2 switching speed (low Ion / Ioff ratio) is higher for strained silicon. Highest voltage gain for the strained silicon channel material with lower transconductance. This is due to strained layer on silicon or silicon germanium layer.

Table 2 Results from fettoy simulator – Device metrics of nanoscale silicon MOSFET with different channel materials

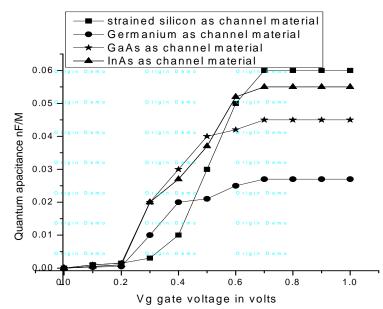
S.No	Output Parameters	Strained Silicon as channel material for silicon nanoscale MOSFET	Germanium as channel material for silicon nanoscale MOSFET	GaAs as channel material for silicon nanoscale MOSFET	InAs as channel material for silicon nanoscale MOSFET
1	Ion	3.273e-003	5.178e-003	6.000e-003	8.826e-003
2	Ioff	1.738e-009	2.255e-009	2.001e-009	1.334e-009
3	Threshold swing (S) mv /dec	59.45	59.51	59.58	59.66
4	DIBL mv / v	1.15	1.15	1.15	1.15
5	Transconductance gm (S / m)	6.565e+003	1.056e+004	1.237e+ 004	1.850e+004
6	Output conductance, gd (S/m)	6.112e-010	1.637e-009	4.507e- 009	3.151e-007
7	Voltage gain at highest gate and drain bias, Av	100e12	645e10	27e12	5.8e10
8	Carrier injection velocity m/s	4.238e+005	6.929e+005	8.473e+ 005	1.629e+006
9	Ion / Ioff ratio	1.88e06	2.2e06	3e06	6.6e06

The mobility of charge carrier in silicon is low compared to the other channel material which gives lower drain current. The strained silicon has threshold swing of 59.45, lowest while comparing other channel materials considered. Hence it is possible to suppress sub threshold parameters in strained silicon.

Gallium arsenide can be used as alternative channel material on silicon wafer. This heterostrucutre nanoscale MOSFET is simulated and results are tabulated in table 2. Gallium arsenide has highest carrier injection velocity due to higher mobility of GaAs material. It has higher on current, transconductance, carrier injection velocity while comparing silicon and germanium with reduced voltage gain. Apart from this, structural defects with silicon is higher to be considered as channel material but with voltage gain and threshold swing which gives Silicon and germanium is better than compound semiconductor materials. We have considered InAs also but the result from table 2 shows that highest threshold swing with lowest voltage gain. Germanium may be considered because of higher on current, transconductance, carrier injection velocity than silicon due to higher mobility and transconductance.

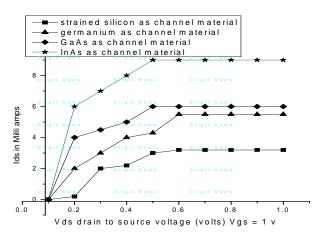
3.1 Qc – Vg Characteristics

Figure 1 shows the quantum capacitance versus gate voltage. The device can be operated at quantum capacitance limit when its gate capacitance is considerably higher than quantum capacitance. To know device operation at QCL limit, value of quantum capacitance and about inversion, depletion accumulation region the study of Qc – Vg curves are drawn. Qc – Vg curve of germanium has low quantum capacitance of 0.025 nf/m with threshold voltage around 0.2 volts. But strained silicon has well defined accumulation and inversion regions with higher threshold voltage due its higher gate capacitance and also quantum capacitance of 0.06 nf/m. GaAs and InAs has low threshold and not well defined depletion regions due its interface state densities. We conclude strained silicon has well defined depletion inversion and accumulation regions with slightly higher theoretical threshold voltage. But germanium curve has lower capacitance and threshold voltage.



quantum capacitance versus gate voltage of different channel material

Figure 1 Quantum capacitance Vs gate voltage of novel channel materials



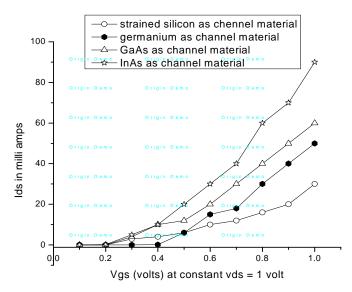
lds vs vds at constant vgs = 1 volt for different channel material

Figure 2 Ids vs Vds at constant Vgs

3.2 Ids –Vgs, Vds Characteristics

Figure 2 and 3 shows the Ids versus Vds at constant Vds of 1 volt, Ids versus Vgs at constant Vds of 1 volt. Exact saturation of occurs around 0.4 volts to 0.5 volts with InAs and GaAs has higher saturation current around 9 and 5 mill amps. Silicon and germanium curves saturates at low drain current and drain voltage. All the curves are simulated at a constant gate voltage of 1 volt. Figure 3 shows Ids- Vgs curve at constant Vds of 1 volt.

InAs and GaAs have higher drain current but it requires lower threshold voltage then it is not possible to suppress subthreshold effects and quantum confinement cannot be achievable. So the germanium and silicon with strained and unstrained materials are preferable for given threshold voltage and optimum drain current. Also higher channel leakage current is possible in GaAs and InAs comparing strained silicon.



IDs vs Vgs at constant Vds = 1 volt for different channel material

Figure 3 Ids vs Vgs at constant Vds

4. Conclusion

This paper discuss about simulation of ballistic nanoscale MOSFET with different channel materials like germanium, strained silicon, InAs and GaAs in fettoy simulator. Strained silicon has higher voltage gain and lowest threshold swing parameters. But germanium has higher on current and better transconductance and moderate switching speed than silicon. Due to strained layer of silicon higher voltage gain is possible and also able to suppress subthreshold parameters. Germanium has better carrier injection velocity. We conclude that strained silicon layer on germanium layer gives less subthreshold effects and can be operated near to quantum confinement regime and also better device metrics comparing to compound semiconductor materials.

5.Reference

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